Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.115”**

**Source**

**G**

**.175”**

**Top Material: Al**

**Backside Material: CrNiAg**

**Bond Pad Size: S = .025” X .034” G = .028” X .026”**

**Backside Potential: Drain**

**Mask Ref: HEX-3 GEN 3**

**APPROVED BY: DK DIE SIZE .115” X .175” DATE: 3/27/23**

**MFG: INT’L RECTIFIER THICKNESS .019” P/N: IRFC430**

**DG 10.1.2**

#### Rev B, 7/19/02